APPLICATIONS OF THE SILICON PLANAR FIELD-EFFECT TRANSISTOR

by Larry Blaser and John S. MacDougall

The characteristics of the silicon planar field-effect transistor make it particularly useful in low-level amplifiers with high input impedance and in certain chopper and attenuator applications where its lack of offset voltage is an advantage. A typical Fairchild silicon planar FET (the 2N3277) has an input impedance of several thousand megohms and a noise resistance of 2 megohms at 1 Kc. The FET is most effectively used in FET-transistor hybrid circuits.

This application note describes some of the characteristics of the device, discusses factors that must be considered in designs utilizing it, and presents several unique and effective hybrid circuits.

Characteristics of the field-effect transistor

The FET resembles the pentode vacuum tube rather than the conventional transistor. Its symbol is shown in Fig. 1 together with a set of typical drain characteristic curves. The drain is equivalent to the anode of the conventional tube, the source to the cathode, and the gate to the grid. As shown in Fig. 1, the characteristic curves consist of two regions:

1. The ohmic region to the left, where the curves are rising. This area corresponds to the saturation region of the transistor.

2. The pinch-off region to the right, where the curves are flat. This is the most useful region for amplification.

For small signals the FET has the simplified equivalent circuit of Fig. 2. The values shown for a typical device (the Fairchild 2N3277) were taken in the pinch-off region. It can be seen that the input is mainly capacitive except for a very large resistance, R_{GS}. The output impedance, R_{DS}, like the plate resistance of a vacuum tube, shunts the current generator, $g_m e_i$, and thus limits the output voltage. There is a small feedback capacitance, C_{DG}, from drain to gate which must be considered in high-frequency design.

DESIGN CONSIDERATIONS

Bias

FET amplifiers are generally connected either in a common-source or a common-drain configuration. The common-source circuit has large voltage gain with moderate stability; the common-drain circuit has less than unity voltage gain, high stability, and maximum input impedance.

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Unlike a transistor, which is normally "off" and must be turned "on", the FET is normally "on" with zero gate voltage and must be turned "off". A small input signal is allowable below the zero bias level but, because of the forward biasing of the gate source diode, the input impedance of the device rapidly becomes non-linear, eventually limiting the signal at approximately -0.6 volts with respect to zero bias. In addition, there is inherent drift of the operating point with temperature. For these reasons the simple bias circuit of Fig. 3a is only marginally useful, and some form of bias stabilization is normally required. Figure 3b shows a circuit with self-bias provided by a source resistor, R_S. Usually R_S will be large enough to limit the voltage gain and must be bypassed as shown. The size of the gate bias resistance is determined by considering it a swamping current drain for the leakage of the back-biased input diode. The size of R_S is determined by considering its feedback effect on the change of drain characteristics with temperature.

Gain

Since the current gain of the FET is very large and difficult to measure and control, the inherent gain of the device is described by a transconductance term, "g_m." The output generator, $g_m e_i$, is shunted by the load resistance, R_L, and by the output resistance, R_{DS}, of the device. Thus for the simple bias circuit with source resistance bypassed or shorted (as in Fig. 3b), the voltage gain is

$$A_v = \frac{g_m R_L R_{DS}}{R_L + R_{DS}} \tag{1}$$

or if $R_L << R_{DS}$, then

$$A_v \approx g_m R_L \tag{2}$$

If the source resistance, R_S, is left unbypassed, then the voltage gain is

$$A_v = \frac{g_m R_{DS} R_L}{(R_L + R_S + R_{DS}) + g_m R_S R_{DS}} \tag{3}$$

And, since R_{DS} is much greater than either R_L or R_S, Eq. (3) reduces to

$$A_v \approx \frac{g_m R_L}{1 + g_m R_S} \tag{4}$$

If $g_m R_S >> 1$, the voltage gain is

$$A_v \approx \frac{R_L}{R_S} \tag{5}$$

In any amplifier configuration the voltage gain of the previous stage or of the generator will depend on the input impedance of the FET circuit. This input impedance will be almost entirely due to the gate bias resistor which, although low compared with the intrinsic input of the FET, does have the virtue of being constant with temperature. The input impedance can easily be raised in a-c amplifiers by adding positive feedback, as shown in connection with the unity-gain amplifier described below.

For the common-drain configuration in Fig. 4, if $g_m R_S >> 1$, the voltage gain will be

$$A_v \approx \frac{g_m R_S}{1 + g_m R_S} \approx 1 \tag{6}$$

Noise

Noise sources in an FET can be represented by noise current generators,

$$\sqrt{\overline{i_{n1}^2}} \quad \text{and} \quad \sqrt{\overline{i_{n2}^2}}$$

in the gate-to-source junction and the source-to-drain channel as shown in Fig. 5. Noise generator $\sqrt{\overline{i_{n1}^2}}$

represents the noise caused by the reverse-biased gate-to-source junction. In planar devices this noise is very small and can be neglected. At low frequencies noise generator

$$\sqrt{\overline{i_{n2}^2}}$$

predominately represents "1/f" noise. At higher frequencies, where 1/f becomes negligible,

$$\sqrt{\overline{i_{n2}^2}}$$

is primarily dependent upon the transconductance of the device and approaches a minimum constant value of

$$\sqrt{\overline{i_{n2}^2}} \approx 4kTBg_m \tag{7}$$

where

k = Boltzmann's constant = 1.38×10^{-23} joules/°K

T = Absolute temperature

B = Power bandwidth

In the FET amplifier of Fig. 6, the small effect of the noise current

$$\sqrt{\overline{i_{n1}^2}}$$

is ignored. The noise contribution of noise current

$$\sqrt{\overline{i_{n2}^2}}$$

is referred to the input of the FET as a noise voltage

$$\sqrt{\overline{e_n^2}}$$

by dividing

$$\sqrt{\overline{i_{n2}^2}}$$

by the transconductance, g_m.

$$\sqrt{\overline{e_n^2}}$$

is independent of source resistance. It is expressed in terms of an equivalent noise resistance, R_n, as follows:

$$\sqrt{\overline{e_n^2}} = \sqrt{4kTBR_n} \tag{8}$$

R_n is easily measured, and typical values for the 2N3277 and 2N3278 at audio frequencies are shown in the graph of Fig. 7. At frequencies above which "1/f" noise is small the following relation holds:

$$R_n \approx \frac{1}{g_m} \tag{9}$$

If R_n and the source resistance, R_S, are known, the noise figure, NF, of an amplifier can be calculated. The NF of the amplifier of Fig. 6 expressed in terms of the voltages

$$\sqrt{\overline{e_n^2}}, \sqrt{\overline{e_{ns}^2}}, \text{ and } e_s$$

is

$$\text{NF (db)} = 10 \log \left[\frac{e_s^2}{\overline{e_{ns}^2}} \div \frac{e_s^2}{\overline{e_{ns}^2} + \overline{e_n^2}} \right] \tag{10}$$

which reduces to

$$\text{NF (db)} = 10 \log \left[1 + \frac{\overline{e_n^2}}{\overline{e_{ns}^2}} \right] \tag{11}$$

But the thermal noise voltage in terms of R_S is

$$\sqrt{\overline{e_{ns}^2}} = \sqrt{4kTBR_S} \tag{12}$$

Substituting Eqs. (8) and (12) in Eq. (11) gives NF in terms of R_n and R_S as follows:

$$NF\ (db) = 10 \log \left[1 + \frac{R_n}{R_S} \right] \tag{13}$$

Thus for the 2N3277 and 2N3278 operated from a 1 M source resistance the NF is typically 2 db at 1 Kc.

APPLICATIONS

As stated above, the FET is most useful in conjunction with other devices. Its best properties are its high input impedance and lack of offset voltage across the output terminals. A number of examples illustrating the design properties of the FET are given below.

Common-source amplifier with emitter-follower

For the simple circuit of Fig. 3b using the 2N3278 a small-signal gain of 10 into a 100-K load is possible. Although this gain may be adequate when several stages are cascaded, the impedance must be reduced for the output stage. The necessary reduction can best be accomplished by using an emitter-follower amplifier as shown in Fig. 8. The gain of this circuit is

$$A_v = \frac{g_m\ h_{fe}\ R_3\ R_5}{R_3 + h_{fe}\ R_5} \tag{14}$$

As large a value of resistance was chosen for R_4 as was possible without limiting the output signal swing. The 100-K resistor selected gives a source voltage of -6 volts with a bias current of 60 μA. Since a gate-to-source voltage of approximately 2 volts is necessary for this bias current, a voltage divider is required at the input. The value of R_2, the lower resistor of the voltage divider, is selected as a compromise between two conflicting requirements: (1) It must be large in order not to shunt the input impedance; (2) it must be small enough so that the high-temperature gate diode leakage current (0.5 μA at 150°C) does not change the bias significantly. For this example a value of 3.3 M was chosen, and the value of R_1 was then calculated to be 15 M. The gain of the circuit of Fig. 8, measured with the values shown, agreed with the calculated value of 10.

Unity-gain amplifiers

The input impedance of 3 M achieved in the circuit of Fig. 8 is not particularly large compared with the inherent input impedance of the FET. To obtain higher values it is necessary to bootstrap the input bias resistors by some circuit like the one shown in Fig. 9. For this configuration the input impedance is greater than the source bias resistor, R_1, as given by the equation

$$R_{in} = \frac{R_1}{1 - A_v} \tag{15}$$

where

$$A_v = \frac{g_m h_{fe} R_4 R_5}{g_m h_{fe} R_4 R_5 + h_{fe} R_5 + R_4} \approx \frac{g_m R_4}{1 + g_m R_4} \tag{16}$$

For a high-impedance circuit the frequency response will be limited by the input capacitance, given by

$$C_{in} \approx C_{DG} + C_{GS} (1 - A_v) \tag{17}$$

Practically, however, C_{in} is usually limited by the stray wiring capacitance.

Another type of unity-gain amplifier which uses feedback to achieve gain stability is shown in Fig. 10. Here the voltage gain is

$$A_v = \frac{g_m h_{fe}' R_4}{1 + g_m h_{fe}' R_4} \tag{18}$$

where

$$h_{fe}' = h_{fe} \left(\frac{R_5}{R_5 + h_{ie}} \right) \tag{19}$$

This circuit is shown bootstrapped by the technique of Fig. 9 to give an input impedance of 300 M and a voltage gain of 0.988.

Attenuator and chopper

As can be seen from the drain characteristics of Fig. 1, the FET will operate

as a low-level switch with an "on" resistance of 8500 ohms and an "off" resistance of greater than 100 M. The "on" resistance is not nearly as low as that obtainable with a transistor, but unlike the transistor the FET has no offset voltage and therefore operation in simple uncompensated circuits is possible down to microvolt levels. Figure 11 shows a simple input to a chopper stabilized amplifier which can operate with signals of 10 microvolts. Input signals up to 5 volts with either positive or negative polarities are possible using special circuits, provided sufficient drive is given to the FET.

It can be seen in Fig. 12 that the characteristic curves of the FET in the nonpinch-off or ohmic region are completely bilateral for small signal levels and have good linear slopes. This fact suggests using the device as a low-level attenuator for agc circuits. The small-signal a-c resistance of the FET was measured and is shown plotted in Fig. 13. Variations of resistance from 8 K to 100 K are possible, the most rapid change occurring at 20 K to 100 K. An application of this idea to an actual circuit is shown in the Wein bridge oscillator below.

Simple analog amplifier

A high-gain amplifier which performs simple analog summing functions and has a minimum of components is shown in Fig. 14. The common-drain FET input is fed to a high-current-gain, low-noise NPN transistor which, with its bias, almost entirely determines the voltage gain of the circuit, as given by

$$A_v = \frac{h_{fe3}R_5R_2(R_3 + R_4)}{R_3R_4(R_2 + h_{fe3}R_5)} \approx \frac{R_2(R_3 + R_4)}{R_3R_4} \qquad (20)$$

The second NPN transistor helps to provide a low-impedance output. The great virtue of this circuit is that the feedback resistor, R_6, provides the bias in addition to determining the input impedance, so that the circuit can be used for a variety of simple analog functions as well as for a simple stable amplifier with a gain of 100. The value of R_6 can be varied at will over the range of 0 to 3.3 M without affecting the bias since almost no current flows at the input to the FET. The use of this amplifier is illustrated by the design of the Wein bridge oscillator described below.

Wein audio oscillator

One of the commonest and most versatile of the RC frequency-controlling techniques used in audio oscillators is the Wein circuit of Fig. 15. This circuit

shows a phase null at the point where $A_v = 1/3$ if the bridge elements are equal. The null frequency is given by the equation

$$f_{null} = \frac{1}{2\pi RC} \tag{21}$$

Fine tuning is usually accomplished by ganging the condensers because they can most easily provide good tracking, but in some commercial instruments it has been done by ganged wirewound resistors. A carbon potentiometer is desirable for this purpose because of its low cost and the possibility of volume production, but it is not normally used in a Wein bridge because its tracking is poor and the output may override the agc circuit. In this design, however, it was used because the agc circuit can control large gain variations.

In the conventional Wein oscillator the frequency-controlling element is used in the bridge configuration shown in Fig. 16. At the null the resistive elements which constitute the voltage-divider part of the bridge are arranged to have nearly the same attenuation as the Wein circuit. Quite commonly one is a power-controlled nonlinear resistor to provide amplitude stability.

Several variations of the Wein oscillator are possible by modifying the method of applying the feedback and inserting the control elements. One of these is shown in Fig. 17a. This is an intriguing circuit because it uses two basically identical amplifiers and because it can easily be modified for amplitude control. The equation relating the two amplifier gains is

$$A_2 = \frac{3 + 2A_1}{A_1}$$

Thus if the gain of $A_1 >> 3/2$ the gain of A_2 is very nearly equal to 2 and almost independent of A_1. The basic amplifier shown in Fig. 14 was used for both A_1 and A_2. For A_1 the circuit of Fig. 14 was used intact, the feedback and bias resistor, R_6, being one of the Wein resistive elements. The second amplifier, A_2, has a gain of approximately 2, which must be varied slightly to set the amplitude of the signal. In order to control the gain of A_2 an FET was used for agc in the modified circuit of Fig. 17b. Resistors R_1 and R_2 reduce the output of the first amplifier to a level of approximately 30 millivolts so that the subsequent FET agc device will not introduce distortion. The FET amplitude-control resistor, R_3, in conjunction with the bias and feedback resistor, R_4, determines the resultant gain of the second amplifier.

The complete circuit of the final oscillator is shown in Fig. 18. The oscillator output is detected by diode D_1 and filtered at the gate of the agc FET, Q_4. The reference for the amplitude control is provided by the rapid change in resistance of the FET 2N3277 as its gate voltage is varied over the range of 2 to 3 volts. The amplitude of the signal can be adjusted with the 20 K potentiometer which changes the pre-bias applied to the FET.

REFERENCES

1. A. van der Ziel, "Thermal Noise in Field Effect Transistors," Proceedings of the IRE, August 1962.

2. "Design with Field Effect Transistors Now?" EEE, March 1963.

3. "What's in the Cards for Field Effect Transistors," Electronic Design, January 6, 1964.

4. "Field Effect Transistors," Electronic Design, April 26, 1963.

ILLUSTRATIONS

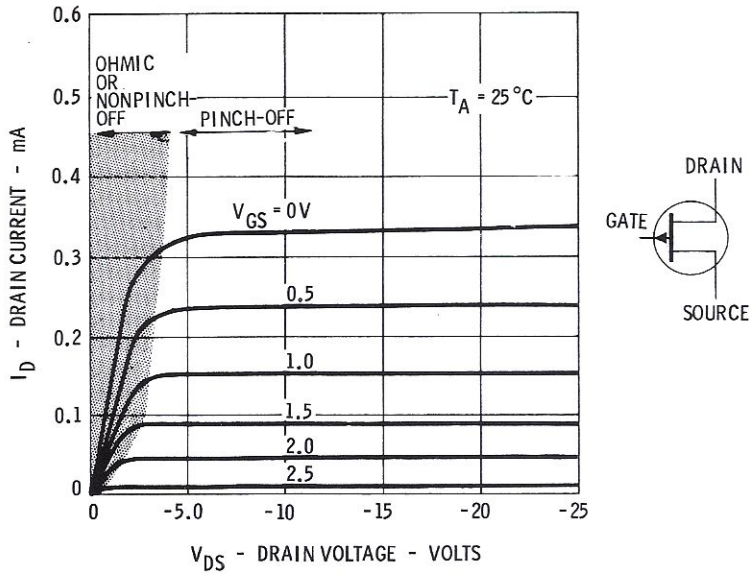


Fig. 1. Drain characteristics of Fairchild 2N3277 P-channel field-effect transistor.

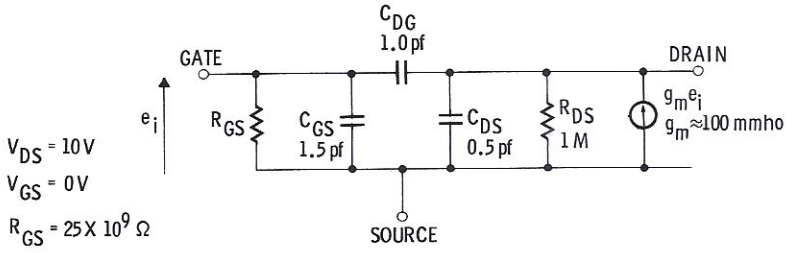


Fig. 2. Simplified equivalent circuit of field-effect transistor for small signals—typical values shown for Fairchild 2N3277.

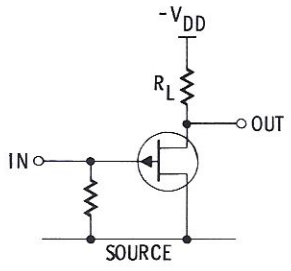


Fig. 3a. FET common-source circuit with simple biasing.

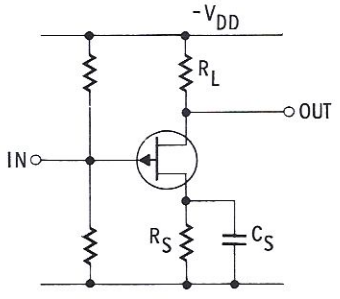


Fig. 3b. FET common-source circuit with stabilized bias.

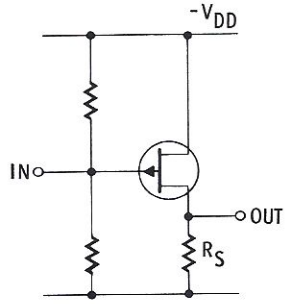


Fig. 4. FET common-drain circuit.

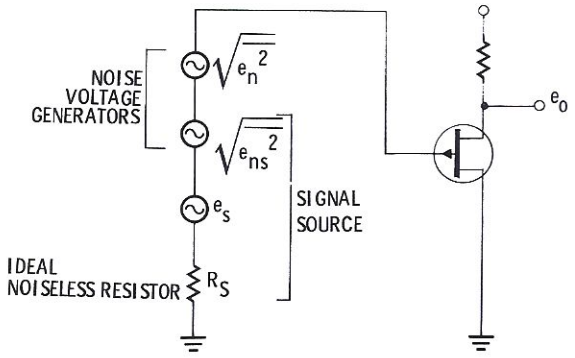


Fig. 6. FET noise characterized by a noise voltage generator at the input.

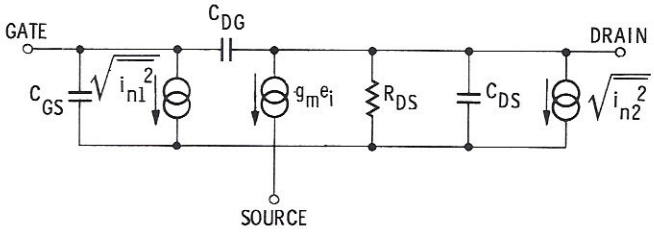


Fig. 5. Equivalent circuit with noise sources represented by noise current generators.

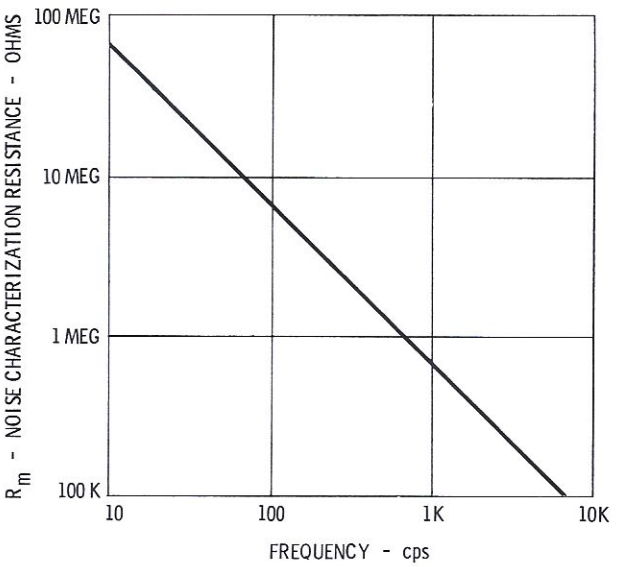


Fig. 7. Noise characterization of the 2N3277 and 2N3278.

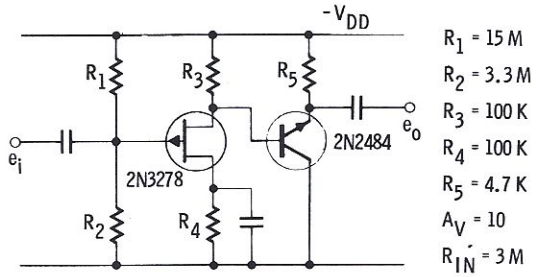


Fig. 8. Common-source amplifier with emitter-follower.

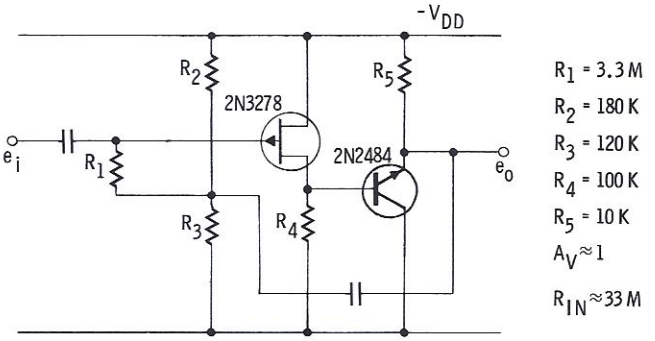


Fig. 9. Bootstrap circuit for very high input impedance.

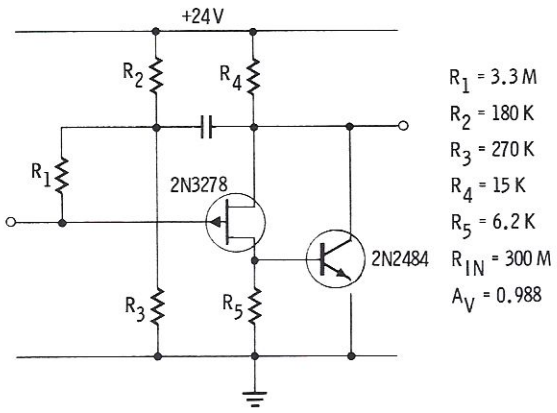


Fig. 10. Accurate unity-gain isolation amplifier.

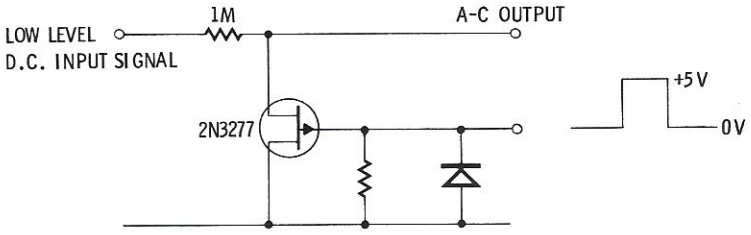


Fig. 11. FET low-level chopper.

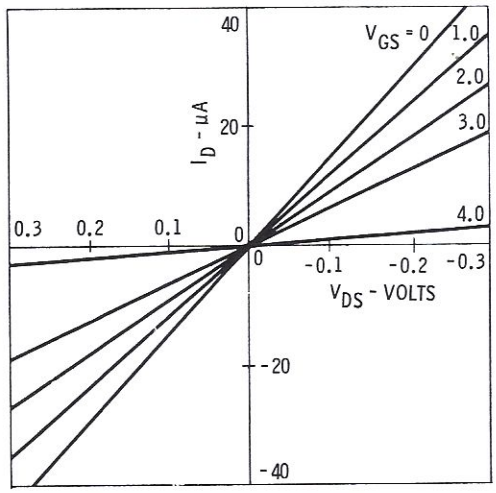


Fig. 12. FET low-level bipolarity drain characteristics for 2N3278.

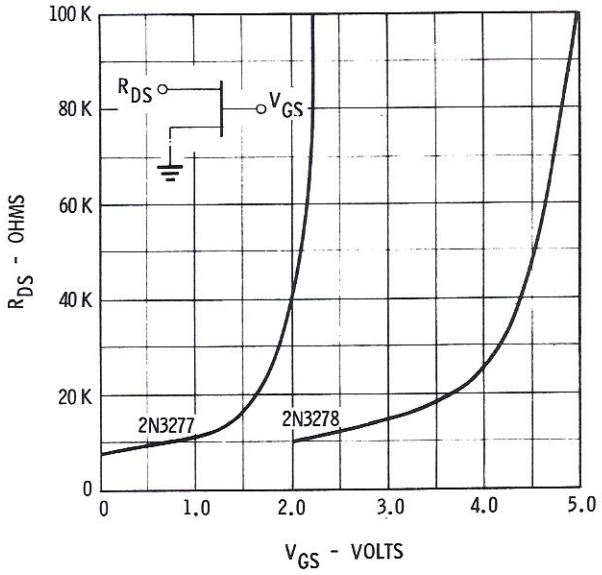


Fig. 13. Small-signal FET resistance variation with applied gate voltage.

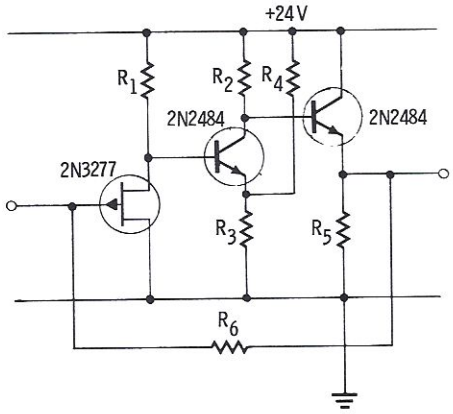


Fig. 14. Simple FET analog amplifier.

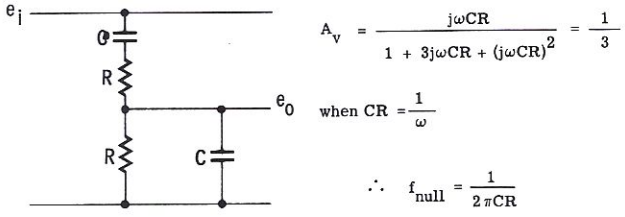
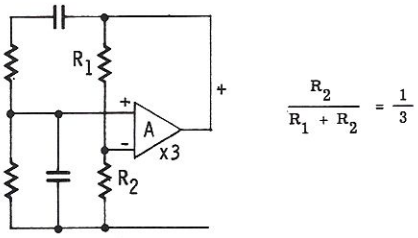
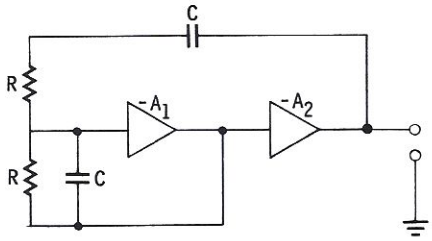


Fig. 15. Wein frequency-determining element.



$$\frac{R_2}{R_1 + R_2} = \frac{1}{3}$$

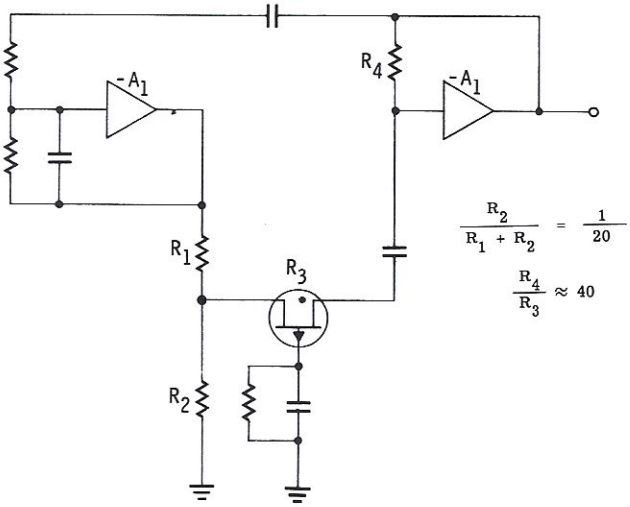
Fig. 16. Conventional Wein oscillator.



$$f_{null} = \frac{1}{2\pi CR}$$

$$A_2 = \frac{3 + 2A_1}{A_1}$$

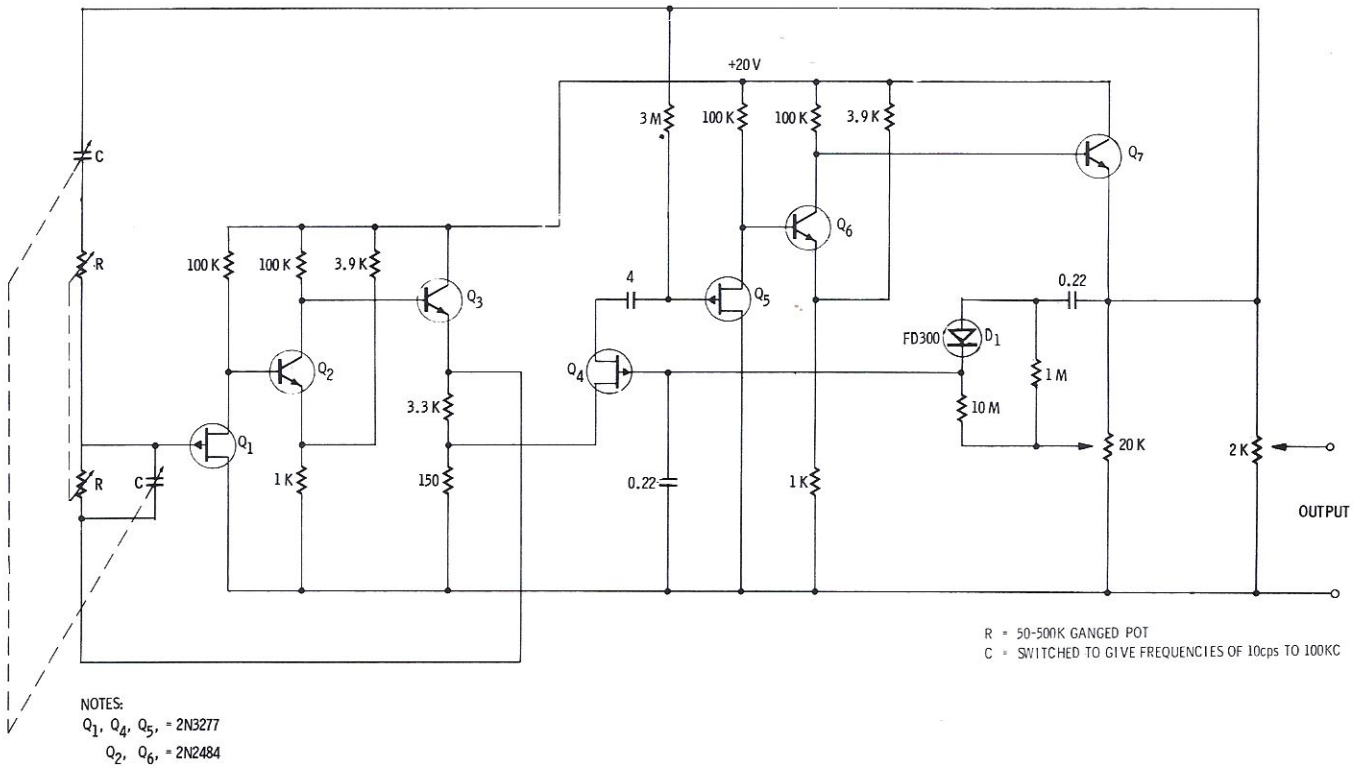
Fig. 17a. Variation of the Wein circuit.



$$\frac{R_2}{R_1 + R_2} = \frac{1}{20}$$

$$\frac{R_4}{R_3} \approx 40$$

Fig. 17b. Circuit of Fig. 17a modified for use with FET attenuator.



NOTES:
Q_1, Q_4, Q_5, = 2N3277
Q_2, Q_6, = 2N2484
Q_3, Q_7, = 2N1711
All resistance values in ohms.
All capacitance values in µf.

Fig. 18. Wein oscillator using FET's.